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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,701	02/11/2004	Hao Fang	2-4	3435

7590 05/10/2006

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EXAMINER	
NEGRON, DANIELL L	
ART UNIT	**PAPER NUMBER**
2627	

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,701	FANG ET AL.	
	Examiner	Art Unit	
	Daniell L. Negrón	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 10-21* is/are rejected.

7)☒ Claim(s) *7-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on February 11, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 3 and 14, claims 3 and 14 are unclear as to how the claimed circuit is configured having a ***"combination"*** of transistors since in independent claims 1 and 11 Applicant regards the circuit as having "***a* [single] *transistor***". The limitation set forth in claim 3 is being interpreted as a circuit having a transistor comprising one of a PMOS and NMOS transistor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 and 10-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leighton et al U.S. Patent No. 6,512,646 in view of Price Jr. U.S. Patent No. 6,184,727.

Regarding claims 1-6, Leighton et al disclose an impedance match write circuit (Fig. 5) comprising an interconnect (11) for connecting to a write head (10), at least one resistor (R_{PA1}, R_{PA2}) between a control voltage (V_{CC}) and the interconnect for impedance matching to the interconnect.

Leighton et al further disclose transistors (Q_7, Q_8) connected to shunt at least a portion of current that would otherwise pass through the at least one resistor during an overshoot mode before the current is in steady state mode (column 5, lines 7-42), but fail to explicitly show the transistor being connected across the element being shunted.

Price Jr. however, discloses a transistor M_4 connected across the write head for the purpose of shunting so current does not pass through the head during an overshoot mode (Fig. 2, column 1, lines 36-43, and column 3, lines 49-52).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the impedance match write circuit disclosed by Leighton et al with the disclosure of a shunt transistor across a write head in order to obtain an impedance matched write circuit wherein write current is bypassed through a transistor during current overshoot for enhanced write circuit current switching.

Regarding claims 2-6, Leighton et al disclose an impedance match write circuit comprising all the limitations of claim 1 as discussed above but fail to explicitly show the details of the shunt transistor as recited in claims 2-6.

Price Jr. however, discloses a PMOS transistor M_4 (column 4, line 61 through column 5, line 10) connected across the write head for the purpose of shunting so current does not pass through the head during an overshoot mode (Fig. 2, column 1, lines 36-43, and column 3, lines 49-52). Transistor is further controlled by a gate voltage source (26) by a V_{PGATE} signal such that the transistor is turned on in an overshoot mode and off in a steady state mode (column 4, lines 61-66).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the impedance match write circuit disclosed by Leighton et al with the disclosure of a shunt transistor across a write head in order to obtain an impedance matched write circuit wherein write current is bypassed through a transistor during current overshoot for enhanced write circuit current switching.

Regarding claim 10, Leighton et al disclose an impedance matched write circuit comprising a first current source at a first side of the interconnect (11) when a voltage at the first side of the interconnect is low (I_1), and a second current source (I_2) at a second side opposite the first side of the interconnect when a voltage at the second side of the interconnect is low (see Fig. 5 and disclosure thereof).. Furthermore, see first and second current sources I_7 and I_8 in Fig. 6 and disclosure thereof.

Regarding claims 11-16, claims 11-16 have limitations similar to those treated in the above rejections of claims 1-6, and are met by the references as discussed above.

Regarding claims 17-21, method claims 17-21 are drawn to the method of using the corresponding apparatus claimed in claims 1-6. Therefore method claims 17-21 correspond to apparatus claims 1-6 and are rejected for the same reasons of obviousness as used above.

Allowable Subject Matter

6. Claims 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 7-9, prior art fails to disclose an impedance matched write circuit as disclosed in claim 1 further wherein the gate voltage source comprises a resistor between a source and a gate of the transistor and a current source from the gate to a negative supply voltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniell L. Negrón whose telephone number is 571-272-7559. The examiner can normally be reached on Monday-Friday (8:30am-5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne R. Young can be reached on 571-272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN
April 24, 2006

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER